RECONFIGURABLE NATO IV RF FRONT-END FOR SDR TERMINALS

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indra

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INTRODUCTION

- **Scope**:
  - Development of a NATO IV RF Front-End (complete development cycle):
    - ***Motivation → Technical Specification → Design → Simulation →*****Iterative** ***Implementation → Integration → Testing***

- **Motivation**:
  - Identification of **NATO IV Band** (4.4 – 5 GHz) as future target frequency band for military systems → LOS/NLOS, PtP/PMP and access deployments scenarios.
  - Emerging SDR platforms allows cost-effective introduction of WFs in this band.

- **Main Drivers**:
  - **Driver I**: Ease integration with any SDR-based digital Base Band unit.
  - **Driver II**: Challenging RF specification, for supporting legacy and innovative state of the art waveforms
  - **Driver III**: Integration in a specific ruggedized enclosure for vehicular platform (MIL-STD 461 and MIL-STD 810 compliant).
    - ***First integration trials*** *→ WiMAX technology (Reference WF) – IEEE 802.16e compliant.*

- **Research Context**:
  - Research and development performed in the scope of a EUREKA project titled **BroadPro** (Broadband Technologies for Professional Applications).
  - Co-funded by Spanish National Authority **CDTI** and **Indra**.
  - Collaboration of the Technological Centre **GRADIANT** (co-author of the paper & presentation).

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01 INTRODUCTION

02 REQUIREMENTS AND DESIGN DECISIONS

03 RF FRONT-END ARCHITECTURE

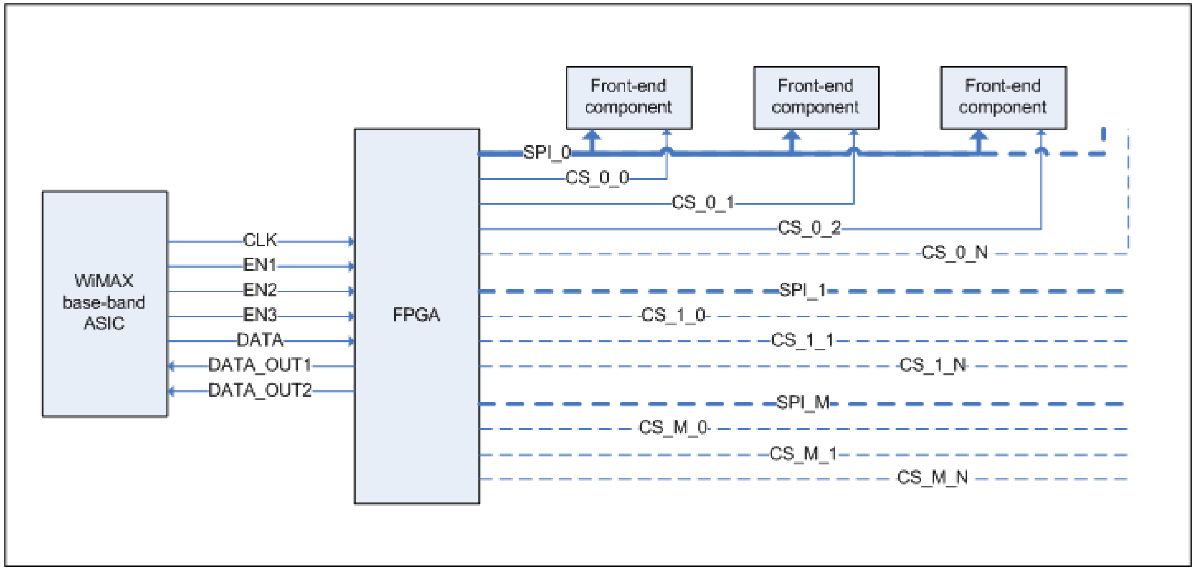
- Hardware Architecture
- Software Architecture

04 IMPLEMENTATION DETAILS

05 CONCLUSIONS

REQUIREMENTS AND DESIGN DECISIONS

- **Driver I: Ease integration with any SDR-based digital Base Band unit.**
  - Flexible RF Front-End control approach is required.
  - Solution based on a FPGA-based proxy capability in charge of:
    - Controlling RF Front-End,
    - Managing RF configuration,
    - Monitoring status of RF Front-End,
    - and providing required interfaces to Digital Subsystem → high density connector with all pins routed to FPGA.
  - ***FPGA FW Architecture***:



- Microblaze soft-core for general functionalities.
- Specific verilog cores for time-constrained functionalities (i.e. AGC operation of frequency switching).
- SPI communication with RF Front-End components.

REQUIREMENTS AND DESIGN DECISIONS (II)

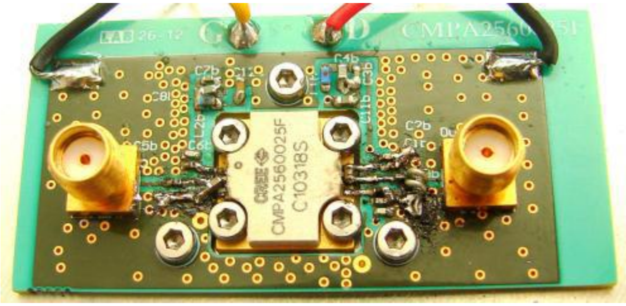
- **Driver II: Challenging RF specification**
  - High reconfigurable **RF channelization**: from 1.5 MHz to 28 MHz
    - Support to narrow band and wide band waveforms.
  - **MIMO** capability
    - Support to WFs that exploit this capacity (increase link capacity)
  - **Transmission power** from -20 dBm up to +24 dBm. (1 dB step configurable).
    - Ease integration of efficient waveform power control algorithms.
    - Max TX power limited by Reference Target WF (WiMAX architecture) and back-off considered (6 dB).
  - **Focus on spectral features:** waveform spectral mask fulfillment, improved installation characteristics (cosite),…
    - **Stringent linearity** requirements in transmitter and receiver:
      - OIP3 greater than +35 dBm.
      - IIP3 greater than +25 dBm.
    - **High Spectral purity**:
      - Spurious rejection level greater than 60 dB.
      - Harmonic rejection level greater than 80 dB.
      - Noise Figure lower than 7 dB.
    - **High Carrier Stability (1 ppm).**
  - **Support to FFH waveforms:**
    - **Fast frequency tuning time** → lower than 80 µs.
    - **Low Phase Noise** → - 114 dBc @ 1 MHz offset from carrier frequency.
    - **Fast and fully reconfigurable AGC:**
      - **Broad Reception Dynamic Range** → 94 dB
        - Support easy integration with narrow band and wide band WFs
      - **Low AGC Attack Time** → lower than 36 µs.

REQUIREMENTS AND DESIGN DECISIONS (III)

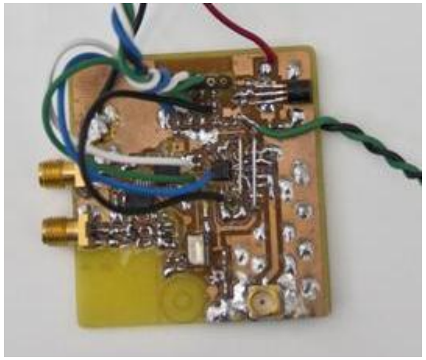
- **Component selection and validation through mock-ups:**

COTS SISO WiMAX Chipset (MAX2838) Mock-up

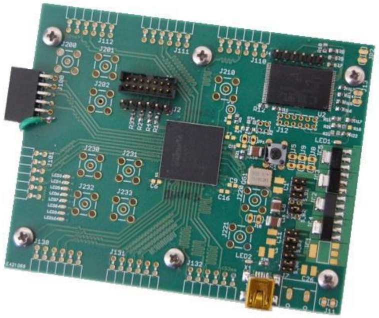
Up-Conversion & Down-conversion Mock-ups



Power Amplifier and adaptation stages Mock-up



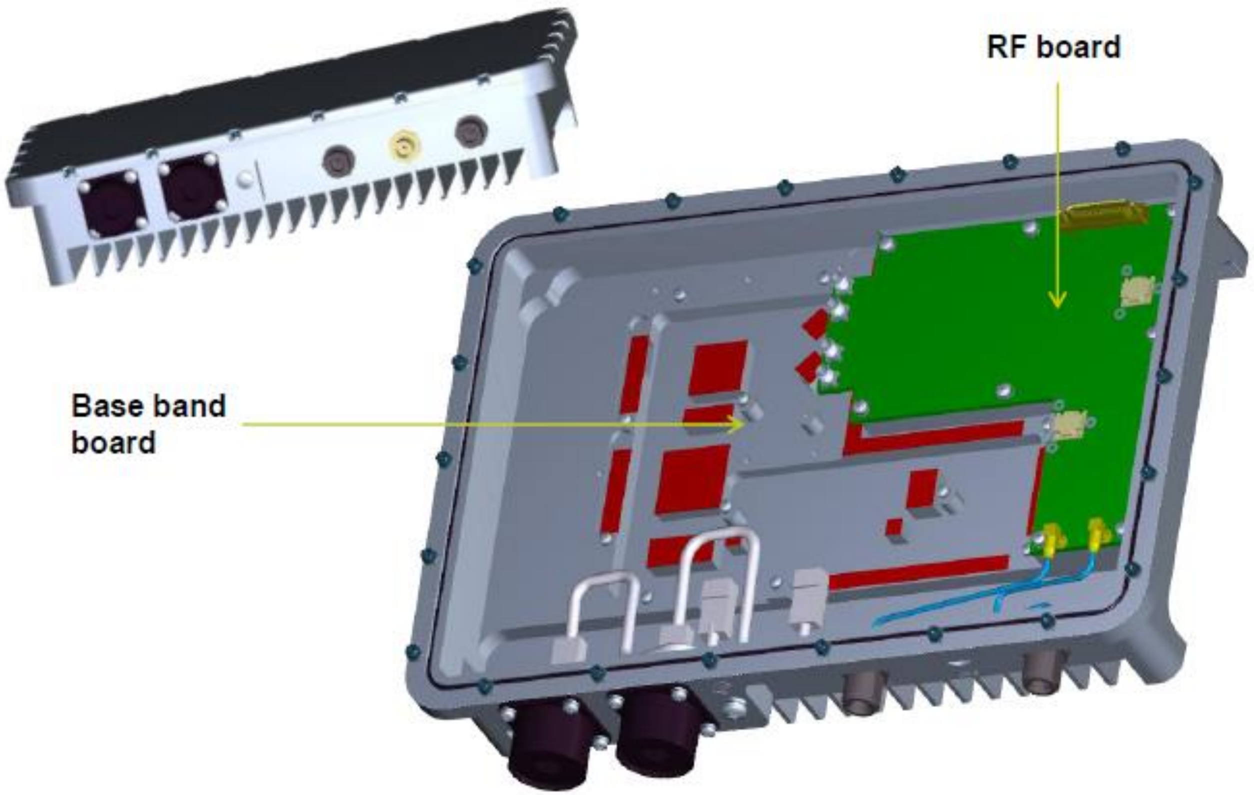
Local Oscillator Mock-up



Control FPGA Mock-up

REQUIREMENTS AND DESIGN DECISIONS (IV)

- **Driver III**: ***Integration in a specific vehicular platform enclosure***
  - RF Front-End HW design restricted by integration in a vehicular ruggedized enclosure.
  - MIL-STD standards compliancy → implies several restrictions.
  - Details at *Implementation Details* section:



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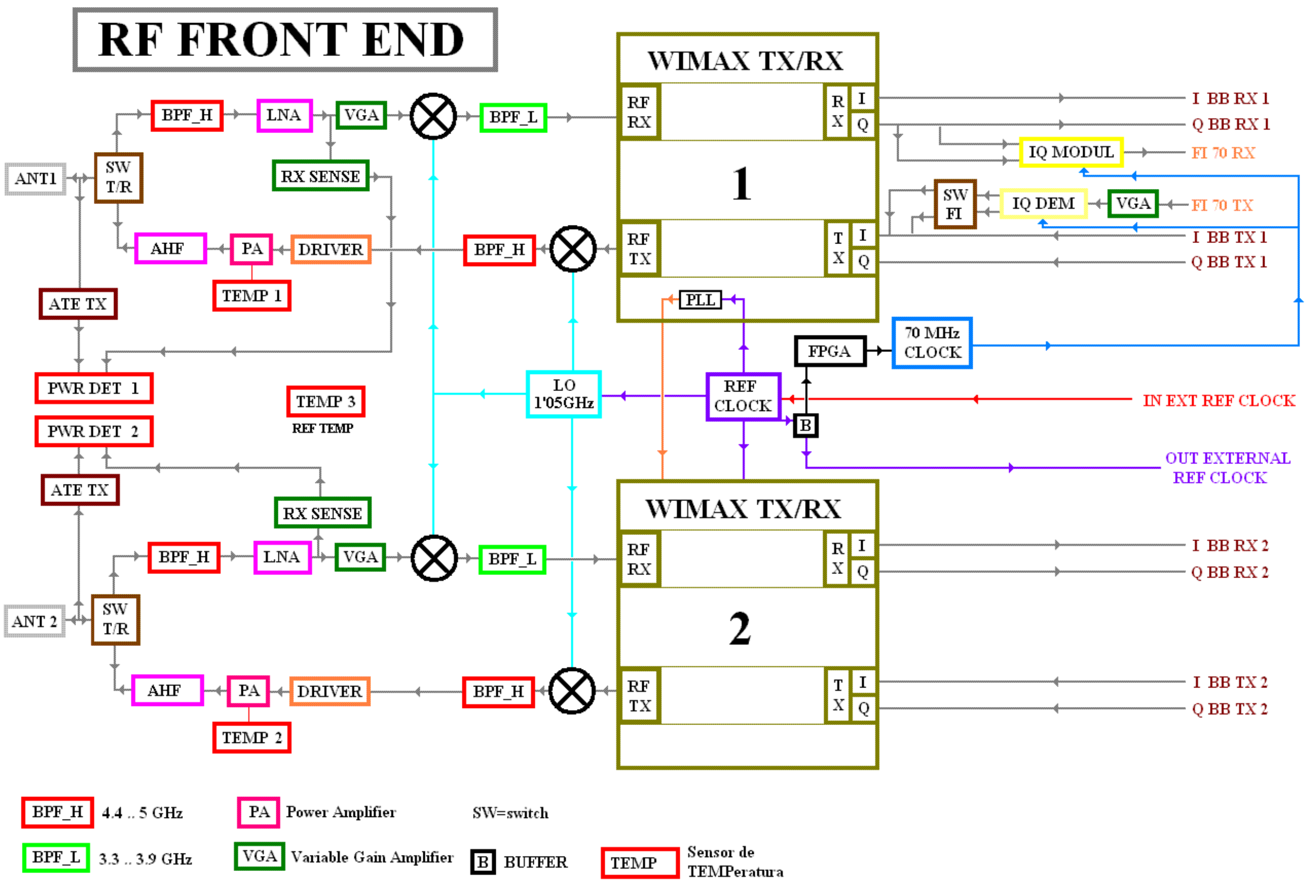
RF FRONT-END ARCHITECTURE

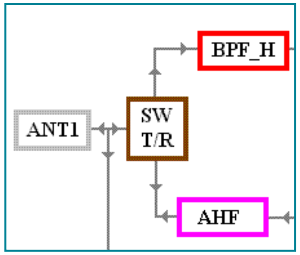
HW architecture Overview:

- Use of commercial WiMAX direct conversion transceivers → **MAX2838** @ 3.3 – 3.9 GHz
- **MIMO architecture** → TX and RX chains duplicated
- **Frequency conversion stage** to move to NATO Band IV (4.4 GHz – 5.0 GHz).

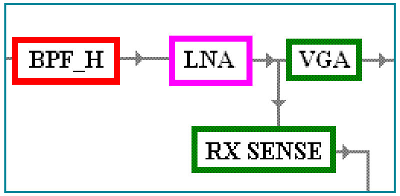


RF FRONT-END ARCHITECTURE (II)

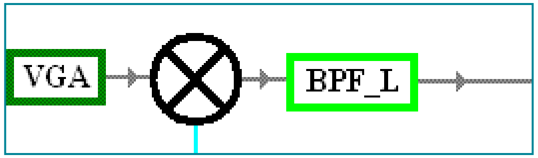
- **HW architecture:** Received Signal Path
  - Two down-conversion branches from NATO Band IV to MAX2838 acceptable band.
  - ***Main components***:
    - **RF Switch.**
    - **Unidirectional High Band Pass Filter:**
      - → Ad-hoc manufactured filters.
    - **Low Noise Amplifier:**
      - → Mini-Circuits Ultra Low Noise MMIC amplifier PMA-5453+
    - **Variable Gain Amplifier.**
    - **Power Detector module:**
      - → Analog Device AD318 Logarithmic detectors.
    - **Mixer:**
      - → SIM-U712H mixers.
    - **Unidirectional Low Band Pass Filter**.



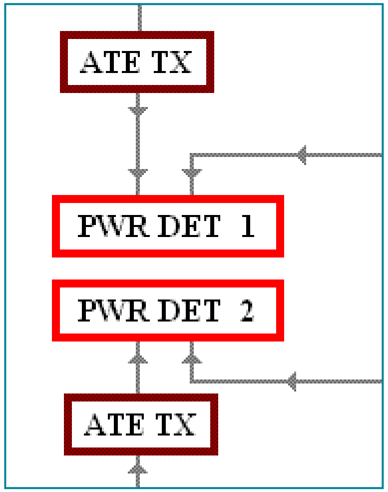
RF Switch



BP filter and amplifiers



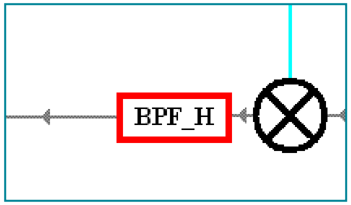
Down-conversion and LP filter



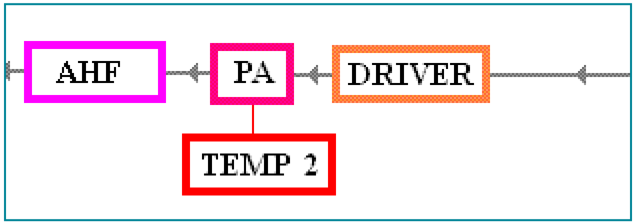
Power detectors: TX & RX Sense

RF FRONT-END ARCHITECTURE (III)

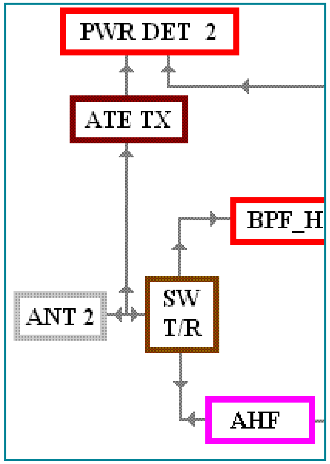
- **HW architecture:** Transmitted Signal Path
  - Two up-conversion branches from MAX2838 native band to NATO Band IV.
  - ***Main components***:
    - **Mixer**:
      - →SIM-U712H mixers.
    - **Unidirectional High Band Pass Filter:**
      - →Ad-hoc manufactured filters.
    - **Pre-Amplification Stage.**
    - **Power Amplifier:**
      - →CREE CMPA2560025F
    - **RF Switch.**
    - **Unidirectional Anti-harmonic Low Pass Filter.**
    - **Power Detector module:**
      - →Analog Device AD318 Logarithmic detectors.



Up-conversion + BP filter



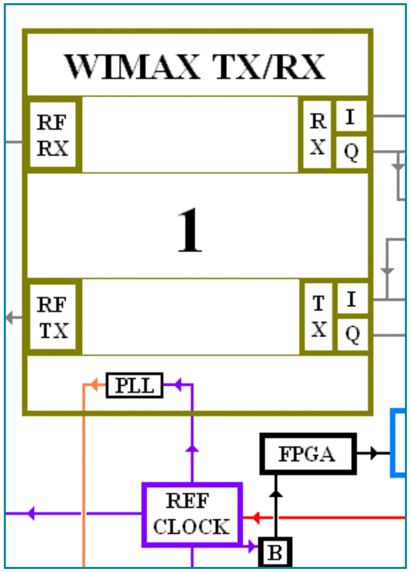
Amplification stage + LP filter



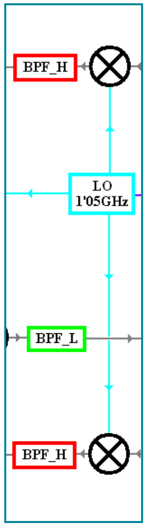
RF Switch + power detectors

RF FRONT-END ARCHITECTURE (IV)

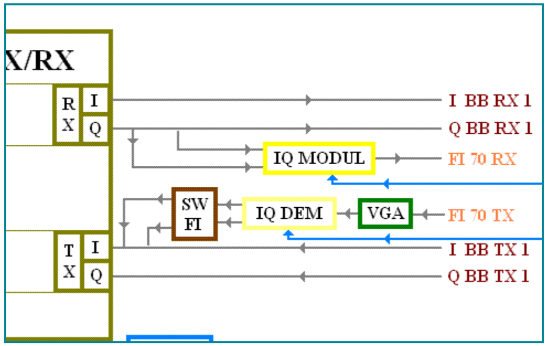
- **HW architecture:** Common
  - **Reference Clock circuit**.
  - **Local Oscillator**:
    - Analog Device ADF4360 VCO + 20 MHz TXCO.
  - **Temperature sensor:** PA & other components
  - **FI Interface**.



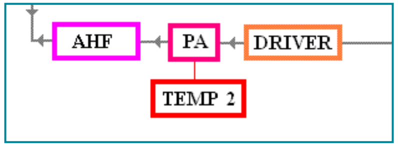
Ref CLK Circuit



Local Oscillator



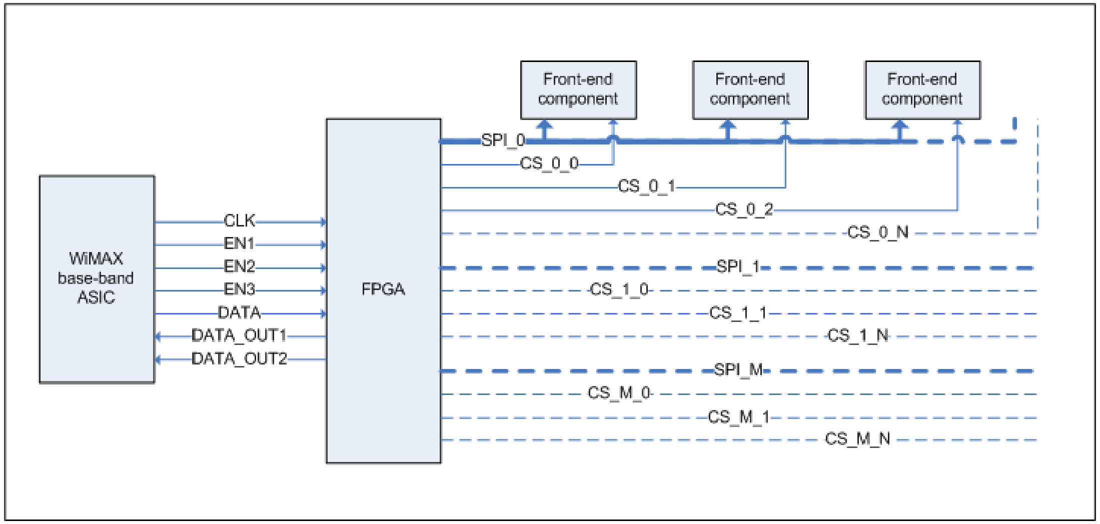
FI Interface



Temp Sensors

RF FRONT-END ARCHITECTURE (V)

- **FW/SW Architecture:**
  - Fully reconfigurable RF Front-End → **FPGA based architecture.**
  - **FPGA XA Spartan-6 family →** extended temperature range (MIL-STD compliancy)
  - **FW FPGA Architecture**:
    - MicroBlaze soft-core CPU processor managing SPI bus between SDR platform and RF-Front-End
    - Also manage SPI buses to other Front-End components:
      - →RF subsystem general control.
      - →OL control.
      - →Transmission power control.
      - → VGAs control with AGC outputs.
      - →ADC for power detection.
      - →AGC parameterization.
      - →Temperature sensors control.
      - →Clock Reference Control.



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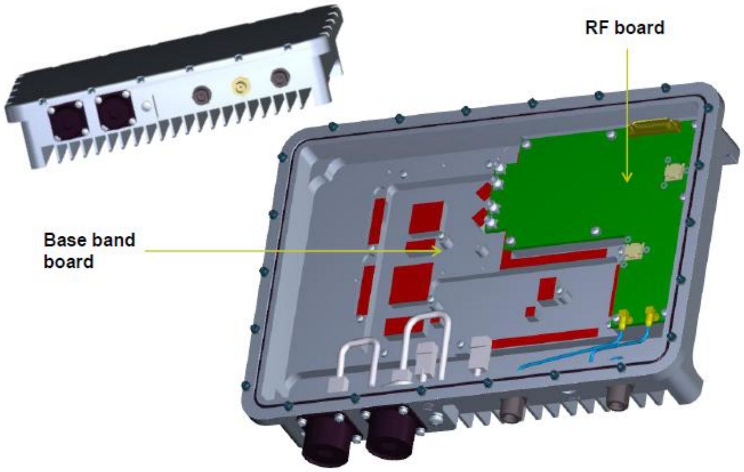
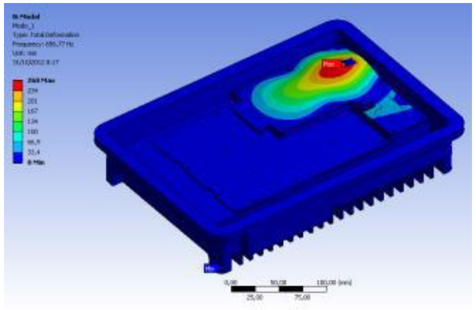
IMPLEMENTATION DETAILS

- Integration of RF Front-End on a **specific vehicular ruggedized enclosure** implies several considerations at implementation phase:

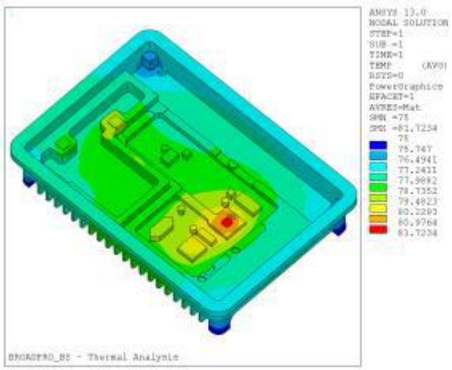


  - **Area restrictions →** restrictions on components selection (i.e. band pass filters).
    - Need for custom implemented components, component reutilization…
  - **MIL-STD compliancy →** specific power dissipation, vibration, shock and stress analysis.

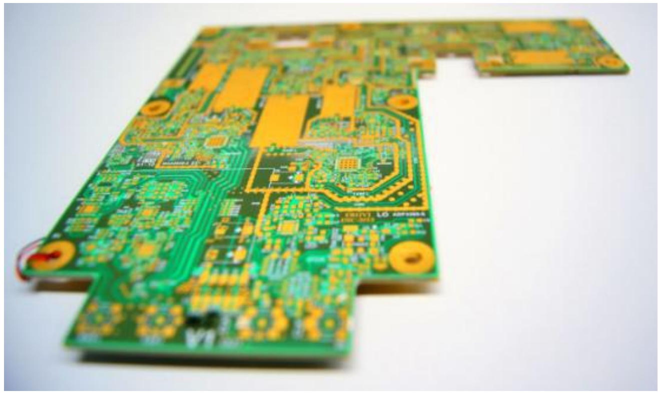


IMPLEMENTATION DETAILS (II)

- **Operational temperature range (-40 ºC to +65 ºC)** → implications on FPGA and PA components and component placing.



- **EMI/EMC requirements, MIL-STD compliancy & area restrictions** → special 6-layer PCB was designed .
  - A full through via hole level, connecting the 6 layers.
  - Top layer for analog RF signals with ground plane.
  - Bottom layer for digital devices and striplines (FPGA, ADCs, power supply for PA, etc…) → noisy devices.
  - Not trivial design → critical via-holes, routing, etc…



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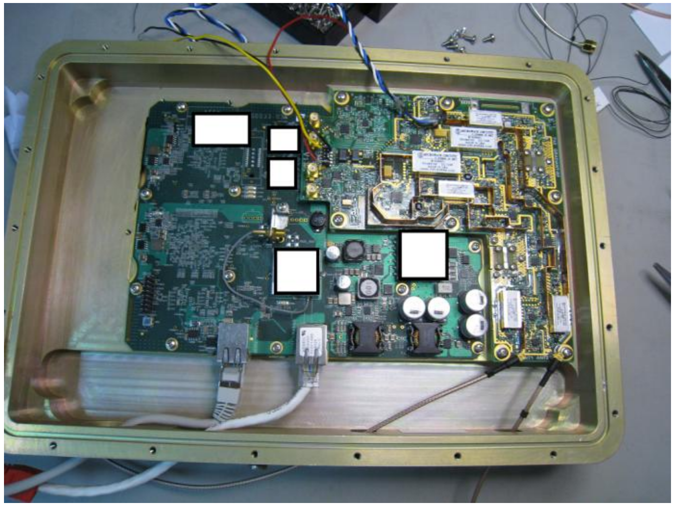
CONCLUSIONS

- **This paper has presented→**
  - Challenges in the development of a fully reconfigurable, multi-mode, SDR-ready and NATO IV capable Front-End.
  - Architectural design decision, components selection and implementation constraints of the RF Front-End.
  - Considerations to allow RF Front-End to be integrated easily with current and future WFs.

- **Feasibility demonstrated →**
  - Implementation and validation of the Front-End for a specific vehicular oriented form factor enclosure.
  - Integration with a digital base band unit WiMAX Standard compliant.



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